Front-end electronics status of CMS electromagnetic calorimeter

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FRONT-END ELECTRONICS STATUS OF CMS ELECTROMAGNETIC CALORIMETER

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ABSTRACT

Compact Muon Solenoid is one of both generic detectors to be constructed for Large Hadron Collider at Cern at the horizon 2005. In the electromagnetic calorimeter subdetector two different parts are foreseen : barrel and endcaps. These are based on $PbWO_4$ scintillating crystals. The scintillation signal is read by avalanche photodiodes in the barrel case and vacuum phototriodes in the endcaps one. A preshower is placed in front of the endcaps. The readout electronics for both photosensors are roughly the same except the preamplifier gain. As electronic circuits will be located just behind the crystal, they must survive a total dose of up to 2 MRad along with 5 E^{13} n/cm^2. The readout chain, designed in radhard technology, consists of a custom dynamic-range floating point preamplifier (FPPA), commercial ADC and custom optical link for each crystal. The design overview and status of this readout electronics for the CMS electromagnetic calorimeter will be presented.

1 Introduction

The CMS Electromagnetic Calorimeter (ECAL) will consist of roughly 80 000 scintillating crystals [1)]. Electromagnetically interacting particles create scintillation light in the crystals proportional to their energy. By measuring the amount of light, and knowing the crystal location, the energy and position of the particle can be reconstructed. The interactions occur every bunch crossing (every 25 ns). The amount of energy deposited in a given crystal during a given bunch crossing is unrelated to the amount deposited during previous or subsequent bunch crossings.

The scintillation light is converted into a photocurrent by a photodetector. In the barrel part of the ECAL (the central cylinder of crystals), each crystal is equipped with two 25mm^2 silicon avalanche photodiodes (APD). The APDs are set in parallel. In the endcaps (the two disks of crystals at the ends of the cylindrical barrel) vacuum phototriodes (VPT) are used. Following the digitizing electronics, digital signal processing circuitry pipelines the data and performs a variety of numerical calculations for use in the experiment trigger. In order to avoid placing this large quantity of digital electronics in the detector radiation environment, to avoid great power consumption and to have enough place for electronics, fiber-optic links, one per crystal, will be used to transport the digitized data off the detector. The on-detector readout thus starts with an optical to electrical conversion and ends with an electrical to optical conversion.

There is a preshower in front of the endcaps. The main aim of this preshower is to provide γ/π° separation in the high η region. It consists of two planes of absorber, constructed from a steel-lead-steel sandwich, each being equipped with an array of 2x2 full-sized silicon microstrip detector (horizontal and vertical layer).

2 System requirements

The Electromagnetic Calorimeter is composed of $PbWO_4$ crystals (see fig.1) located in the 4 T CMS magnetic field. $PbWO_4$ has an intrinsic decay time of roughly 10 ns, and a light yield in full-size crystals of 70 photons/MeV. 85 % of the scintillation light is included in 20 ns. $PbWO_4$ crystals are quasi radiation hard and very compact. The low light yield and high collision

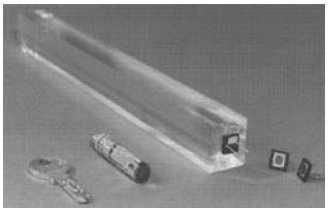

Figure 1: *PbWO4 crystal with VPT and APDs.*

Figure 2: *Capsule device.*

frequency (40 MHz) combined with the need for excellent resolution at energies < 100 GeV requires a photodetector with gain. Such a calorimeter does not need a signal over noise ratio as high as the dynamic range for high energy signals.

The strong perpendicular magnetic field in the barrel precludes the use of vacuum detectors, whereas the high radiation levels in the very forward direction of the endcaps (up to 15 Gy/h) argue against solid state photodetectors ("only" 0.15 - 0.3 Gy/h in the barrel). As a result, the ECAL will use large-area silicon avalanche photodiodes (APD) in the barrel [2] and vacuum photo triodes [3] in the endcaps.

Two APDs of 5 mm $\times$ 5 mm area each are used per crystal, operating at a gain of 50. They are placed in a so-called "capsule" device. A capsule is a molded piece including both APDs, a barcode to follow the capsule in the construction phase and a kapton cable connecting the APDs to the front-end electronics (fig.2).

In the endcaps, the phototriode (see fig.3) has a 22 mm diameter ac-

Figure 3: *VPT sensor.*

Table 1: *ECAL design parameters*

Parameter	Barrel	Endcaps	Units
Full-scale Energy (E, not E_T)	1.5	3.0	TeV
Full-scale Charge	60.0	16.5	pC
Capacitance	< 200	40	pF
Noise Level	10000	3500	e^-
Equivalent Noise	40	100	MeV

tive area, and a gain of at least 6 (in the magnetic field), 8 - 9 is the mean value. At the barrel-endcap division, the photodetectors have a 26 degrees angle with respect to the magnetic field. Some manufacturers have been investigated. The performances of VPT have been checked with crystal array in magnetic fields of up to 3 T in H2 in the CERN North area. The mean VPT electron yield, normalised to a naked crystal light yield of 8 photoelectrons into an Hybrid PhotoMulTiplier, was found to be 25 electrons/MeV for devices from Research Institute Electron, 35 electrons/MeV for devices from Hamamatsu and 20 electrons/MeV for devices Electron Tubes (all devices were 15 degrees to the field). VPTs loose up to 30 % of light when magnetic field increases from 0 to 3 T [4].

Taking into account the spread of crystal light yields and photodetector gains, the full-scale energy in the barrel is set at 1.5 TeV and is 3.0 TeV in the endcaps. In order to minimize complexity in the front-end circuit, energy, rather than transverse energy, is readout. The design parameters are summarized in tab.1.

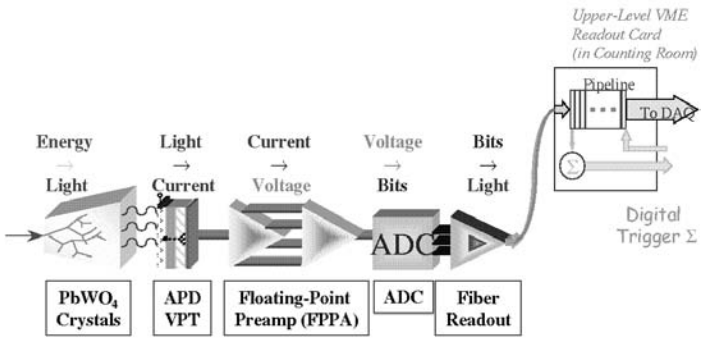

Figure 4: *Light-to-light readout.*

3 Elements of the readout

The readout chain consists of a light-to-light chain as shown in fig.4.

After the rad hard part of the electronics, a fiber optic link transmits, for 10 channels, the data to the upper level readout located in a safe part of the detector. The rad hard part consists, for each crystal, of a so-called Floating Point PreAmplifier (FPPA), a commercial 12 bits ADC, running at 40 MHz and a serializer converting electric signals in optic ones. A control chip is used to set the working mode of a block of ten such channels and to transmit the 40 MHz clock.

3.1 Front-end circuit

The signal capture electronics consists of a custom monolithic floating-point preamplifier [5) 6) 7)] (FPPA) which contains a wide dynamic range (16 bits), low noise, transimpedance preamplifier (conversion of the photocurrent into a voltage) matched to a pair of APDs or a VPT (see fig.5).

The main limitation of a wide dynamic range and high speed photodetector readout chain, when used in a rad-hard environment, comes from the maximum precision of the ADC which is often limited to 12 bits. This drawback could be circumvented by using a compression circuit between the preamplifier and the ADC. The compression technique used in our case, for taking into account the requirement that the ADC resolution must not impair the performance of the system, is a linear multi-gain switching circuit. The 92 dB input dynamic range is thus divided into four ranges of 12 bits each. So, following the preamplifier, are four gain stages, with gains 1, 5, 9 and 33. The gains are

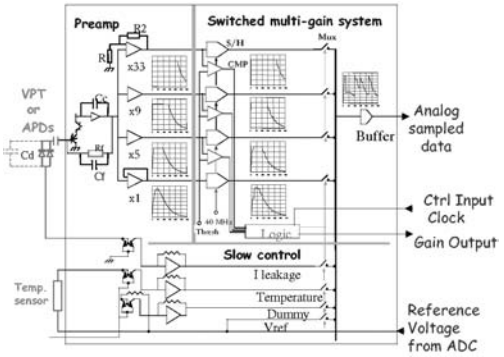

Figure 5: *Block diagram of Floating Point Preamplifier (FPPA).*

fixed by the ratios of internal matched metal resistors which have low thermal coefficients and are radiation resistant. The gain stages have clamps to prevent saturation. The amplifiers have a high closed loop bandwith (250 MHz) followed by matched RC filters which have a typical bandwith of 30 MHz. So the pulse shape is the same for the four ways (variation less than 1 %).

The four channel sampler and multiplexer, which selects the gains and multiplexes them to an ADC, follows the gain stages. It consists of a series of analog switches, comparators and digital logic. Directly after the gain, analog switches are used to form a sample/hold amplifier. Comparators on the three highest gain stages along with digital logic determine which gain stage has the largest, non-saturated signal and multiplex that signal to the ADC via the output buffer. The digital logic also outputs a code indicating which gain range was used. When switched in range 33, the noise coming from the APD and the preamplifier dominates compared to the value of the ADC quantum while when switched in range 1, the quantization noise of the ADC dominates. For normal data taking, the circuit operates in automatic mode and samples the waveform as described above. In addition, a "force" mode is foreseen to select any of the four ranges, especially for gain calibration procedure. Theses modes are selected by four unlatched digital lines.

Two auxiliary inputs allow the readout of an external temperature sensor and photodetector leakage current. The temperature input is matched for a 100 kΩ at 25°C thermistor. A high value resistance was chosen to reduce self

heating. An internal dummy channel is used to control the baseline voltage variation during operation under irradiation. This channel connected to an internal metal resistor is also implemented to be able to distinguish if an output voltage variation comes from a change of temperature or from irradiation effect on the readout chain. The current readout circuitry monitors and converts the leakage current of the APDs from 100 nA to 20μA into a voltage. In addition, the internally buffered and distributed voltage coming from the ADC reference voltage is also monitored.

Sensitive analog parts and digital block are individually surrounded by a dielectric trench for reducing crosstalk. This chip will equip the barrel and endcap part of the CMS electromagnetic calorimeter, by changing the metal mask while keeping the same silicon front-end.

The chip has been tested under 64 MeV protons beam irradiations (at Paul Scherrer Institute). A total dose of 10^{13} protons/cm^2 was applied. A change of preamplifier gain of 0,3 % was observed while no change in shape occured.

The FPPA is followed by a 40 MHz 12-bit ADC (Analog Devices AD9042). Both the FPPA and ADC [8] are fabricated in dielectrically isolated, full complementary bipolar processes. In normal detector operation the peak sample and its two neighbors will be summed to reconstruct the energy deposited in crystals.

3.2 Fiber-optic transmitter

A 10-crystal unit is serviced by one 12-fiber ribbon: 10 fibers transport data off the detector at high speed, and the two remaining fibers are used to bring the LHC bunch crossing clock and a slow serial interface to the detector.

The fiber readout system consists of several elements: the high-speed transmitters and receivers which send data for each crystal off the detector, the lower-speed transmitters and receivers which send the clock and configuration data to the detector, the electro-optic elements, the connectors and the fiber itself. The high-speed transmitter and clock receiver are custom developments due to the radiation environment in the ECAL. In addition, the large number of channels requires a low power design ($<$ 300 mW per transmitter). The remaining components are commercial. To minimize cost, standard 62.5μ/125μ multi-mode fibers with 850 nm VCSELs are used. The high-speed

receiver, being off-detector, can be a commercial part, so the line encoding protocol should correspond to a commercial standard. The protocol transfer is the Agilent's CIMT (Conditional Invert, Master Transition) [9] used in the G-Link. CIMT protocol is simpler to implement and is better suited to the synchronous, continuous environment as synchronization loss is more rapidly and reliably detected. 20 bits are required to transmit a 16-bit word. A fiber-optic transmitter meeting the radiation and power requirements has been constructed in CHFET (Complementary Heterostructure FET) GaAs technology [10]. The design aims for a single-chip solution, with serializer, protocol encoder and VCSEL driver on the same chip. A first proof-of-principle version [11] was submitted in November 1997. This circuit consisted of a 20-bit serializer, converting 20 parallel inputs with a 40 MHz word rate into an 800 MB/s optical output stream. The circuit consumed considerably less power than the maximum allowed (90 mW including VCSEL at 800 MB/s) but suffered from extreme electrostatic discharge (ESD) sensitivity and asymmetry in the VCSEL output. An improved version, which included 16-bit G-Link protocol was submitted in February 1999. The circuit, contains 6108 transistors and is 12 mm^2.

In addition to the choice of encoding protocol, an additional design consideration was the clocking scheme used to accomplish serialization. Conventional serializers employ phase-locked loops (PLLs) to multiply the word clock (40 MHz in this case) up to the serial bit rate (800 MB/s in this case). The serializer then consists of a multiplexer/flip-flop chain running at the bit rate. A PLL-based approach has two potential drawbacks in the ECAL: a potentially higher rate of synchronization loss due to single-event effects in the PLL and potentially higher power consumption due to the high-speed flip-flops. For those reasons, this design uses a delay-locked loop (DLL) rather than a PLL. A PLL consists of a voltage controlled oscillator, divider and phase/frequency detector. The DLL consists of voltage controlled delay elements and a phase detector. In the DLL circuit, only the final OR gate must work at 800 MHz (see fig.6), all other parts run at 40 MHz. For this reason, power consumption is very low.

The complete circuit operating at 800 MB/s dissipates $\sim$ 120 mW.

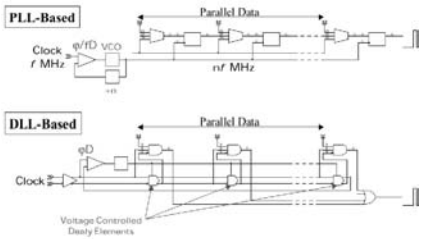

Figure 6: *PLL-Based and DLL-Based serializers.*

3.3 Clock and control circuit

The 40 MHz LHC clock and some configuration data must be transported to each 10-channel readout unit. The readout configuration consists of programming the operating mode of the FPPAs and asserting or de-asserting the line that forces the serializers to send synchronization frames. The FPPAs and serializers are identically programmed in parallel. A circuit accomplishing these tasks has been fabricated in DMILL BiCMOS SoI technology. The 10 mm^2 chip has two p-i-n diode inputs, one carrying the clock and the other carrying a serial data stream.

4 Test in H4 beam

The chain has been tested in H4 beam at CERN during summer 2000. The prototype matrix had 30 channels, with 30 final crystals, final alveolae, final mechatronics and final electronics (serializer excepted). So 3 electronic blocks of ten channels each have been tested.

Fig. 7 shows one card of 5 channels (2 such cards form an electronic

Figure 7: *Electronic card for 5 channels.*

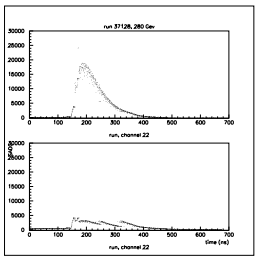

Figure 8: *Reconstructed pulse (above) and raw data (below).*

block). FPPA is the first circuit, then AD9042 appears, the serializer and the optic fiber link (10 data fibers, 1 clock fiber, 1 control fiber).

Fig. 8 shows a typical reconstructed pulse obtained with 3 different gains. Raw data (before reconstruction) is shown under reconstructed pulse. Gains intercalibration was obtained in electronic card "force" mode.

5 Preshower electronics

After the 1999 tests of preshower in the H4 beam at CERN [12], electronics improvements have been decided. Due to noise contributions it has been decided to separate control electronics (digital) and the memory (analog) : the PACE circuit, minimizing the effects of digital crosstalk into the analog preamplifiers.

The readout of silicon detectors used to measure energy deposition in electromagnetic showers presents a number of challenging design issues for the ASIC circuit designer. For the CMS Preshower detector these include a detector loading capacitance of more than 40 pF, peaking time of 25 ns, dynamic range from 0.4 fC to 1600 fC of input charge, S/N ratio better than 10 and radiation hardness. The Delta [13] amplifier has been designed to meet these requirements and has been manufactured as a BiCMOS ASIC chip in the DMILL technology. A new version of the DELTA circuit (front-end charge preamplifier with leakage current compensation and switched gain shaper) has been received in October 2000. A DMILL version of the analog memory (36×160 cells) will be submitted before end 2000. This memory is necessary due to trigger delay. Preshower has no direct trigger but waits for a drawback from trigger units in control room, so data must be pipelined. Only triggered data are sent to the

40 MHz ADC.

6 Conclusion

Final version of different chips involved in CMS ECAL front end will be soon available. First preproduction runs are foreseen for year 2001. In case of producer problems, backup solutions are being developed. Photosensors are chosen and production begins, too. Detector construction is on the way.

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